WHAT IS CLAIMED IS:

1. A multi-layered packet processing device, comprising:

an interface of a public network for transmitting a data packet to a node and receiving the data packet from the node through the public network; and

a plurality of packet processing portions for sequentially processing the data packet in a pipeline pattern, according to a header of the data packet transferred from the interface of the public network.

2. The multi-layered packet processing device of claim 1, wherein the plurality of packet processing portions comprise:

a packet separating processor for outputting a packet to be analyzed, by sequentially including a tag in part of the data packet transferred from the interface, the packet separating processor for storing a remainder of the packet to be analyzed, which is left after the packet to be analyzed is output;

a plurality of header analyzing processors for sequentially analyzing the packet to be analyzed transferred from the packet separating processor, according to a header encapsulated in the packet to be analyzed, and then reflecting an analyzed result in the tag of the packet to be analyzed, and outputting an analyzed packet;

a packet reassembling processor for requesting the remainder of the packet to be analyzed stored in the packet separating processor, when the packet reassembling processor receives the analyzed packet output from the plurality of header analyzing processors, and outputting the analyzed packet together with the

requested remainder of the packet to be analyzed, as a complete data packet; and

an output processor for determining an output route of the complete data packet by analyzing output route information reflected in the tag of the complete data packet transferred from the packet reassembling processor, and outputting the complete data packet according to the determined output route.

3. The multi-layered packet processing device of claim 2, wherein the packet separating processor reassembles asynchronous transfer mode (ATM) cells transferred from the interface.

4. The multi-layered packet processing device of claim 3, wherein the output processor segments the complete data packet transferred from the packet reassembling processor into the ATM cells, and outputs the ATM cells.

5. The multi-layered packet processing device of claim 2, wherein the plurality of header analyzing processors comprise:

an internet protocol (IP) header analyzing processor for determining whether a destination address of the packet to be analyzed matches a system address, and outputting an IP header-removed first packet when the destination address of the packet to be analyzed matches the system address;

a protocol transmission type header analyzing processor for analyzing a protocol transmission type header of the IP header-removed first packet, reflecting the analyzed result in the tag of the packet to be analyzed, and outputting a second packet from which the protocol transmission type header is

removed; and

a lookup processor for updating the destination address of the packet to be analyzed, which is transferred from the protocol transmission type header analyzing processor, outputting an updated packet to be analyzed to the packet reassembling processor, and outputting the second packet, which is transferred from the protocol transmission type header analyzing processor, together with a bypass signal, without processing.